REMARKS

The Office Action mailed on October 21, 2002, has been received and reviewed. Claims 1-20 and 32-71 are currently pending in the above-referenced application. Each of claims 1-20 and 32-71 stands rejected.

Reconsideration of the above-referenced application is respectfully requested.

Rejections Under 35 U.S.C. § 112, First Paragraph

Claims 1-11, 32-38, and 68-71 stand rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention. In particular, each of claims 1-11, 32-38, and 68-71 has been rejected for reciting a structure that includes an intermediate conductive layer that contacts a structure located *beneath* a silicon-containing dielectric layer of a semiconductor device.

The term "beneath," as used in independent claims 1 and 32, was intended to indicate that the structure which is contacted by the intermediate layer is located at a lower level than a silicon-containing dielectric layer of a semiconductor device. Accordingly, claims 1 and 32 have been amended to more clearly recite the relative positions of the contacted structure and the silicon-containing dielectric layer. As the amendments to claims 1 and 32 are being made merely for the sake of clarity, these amendments do not affect the scope of the subject matter recited in either claim 1 or claim 32.

It is respectfully submitted that the amendments to claims 1 and 32 are fully supported by the as-filed specification (*see, e.g.,* FIGs. 2, 3, and 9-11) and, therefore, do not introduce new matter into the above-referenced application.

It appears that claims 2-11, 68, and 69 were rejected primarily on the basis of their dependencies from claim 1, while claims 33-38, 70, and 71 were rejected merely for depending from claim 32.

In view of the foregoing, it is respectfully requested that the 35 U.S.C. § 112, first paragraph, rejections of claims 1-11, 32-38, and 68-71 be withdrawn.

Rejections Under 35 U.S.C. § 102(e)/103(a)

Claims 1-6, 8-10, 32-38, and 68-70 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 5,792,594 to Brown et al. (hereinafter "Brown") or, in the alternative, as being rendered obvious by Brown under 35 U.S.C. § 103(a).

A claim is anticipated under 35 U.S.C. § 102 only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

M.P.E.P. § 706.02(j) sets forth the standard for a section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Brown describes a method for repatterning semiconductor dice for use in flip-chip applications, as well as various products of the method. The method disclosed in Brown includes forming a first dielectric polymer layer on a dielectric layer of a semiconductor die that laterally surrounds and is located in the same plane as bond pads of the semiconductor die. The bond pads are then exposed through the first dielectric polymer layer. Next, a second dielectric polymer layer is formed over the first dielectric polymer layer, and the bond pads and areas of the first dielectric polymer layer upon which circuit traces are to be carried through the second dielectric polymer layer are exposed through the second dielectric polymer layer.

The first dielectric polymer layer use in the method that is described in Brown includes a catalyst. A catalytic metal is also deposited onto the exposed bond pad. The catalyst of the first dielectric polymer layer and the catalytic metal of the exposed bond pad facilitate copper plating

of the first dielectric polymer layer and of the bond pad. The exposed portion of each bond pad and the exposed portions of the first dielectric polymer layer are then plated with a metal, such as copper, that has better conductivity properties and is less corrosive than aluminum. Upon patterning the metal plating, conductive lines and contact pads are formed.

In one described example of the resulting semiconductor die, which is shown in FIG. 4, the new contact pad is formed directly above the corresponding bond pad 12 and is separated from the active surface of the semiconductor die by the two dielectric polymer layers 14, 18. The bond pad 12 is depicted as being located at the same level as and laterally surrounded by a dielectric layer 11, which may be formed from a variety of silicon-containing materials, such as silicon nitride, silicon dioxide, or a glassified surface. As depicted, neither the upper, copper layer 26 or the lower, nickel layer 22 of the new contact pad contacts the silicon-containing dielectric layer 11. Brown does not describe that the formed structure is useful for anything other than to produce a precision interconnecting pattern and terminal bump pattern from metals other than aluminum so as to enhance the performance of a semiconductor die. Col. 2, lines 46-49 and 55-57.

Independent claim 1, as amended and presented herein, recites a contact that includes an intermediate conductive layer, an insulator component positioned "so as to at least thermally insulate [a] structure" of the semiconductor device, and an electrically conductive contact layer. The intermediate conductive layer of amended independent claim 1 contacts and is in electrical communication with *the structure*, which *is located at a lower level than* a silicon-containing dielectric layer of the semiconductor device.

While it is acknowledged that Brown, at col. 4, lines 63-67, teaches that "pads 12 . . . may be located anywhere in an integrated circuit . . .," this blanket statement does not amount to a description, teaching, or suggestion by Brown of pads 12 that are located at a lower level of a semiconductor device than the silicon-containing dielectric layer 11 thereof. Rather, the relevant description of Brown, as shown in FIG. 4 thereof, is limited to a semiconductor device structure that includes a contact that is positioned adjacent to a pad 12 which itself is located at the *same level* as dielectric layer 11 of the semiconductor device. Thus, Brown does not teach, suggest, or expressly or inherently describe a contact that contacts a structure located *at a lower level than* a

silicon-containing dielectric layer of semiconductor device, as is recited in claim 1, as proposed to be amended.

Moreover, Brown lacks any teaching, suggestion, or express or inherent description that the insulator component of the contact thereof may be positioned so as to thermally insulate an underlying structure of the semiconductor device.

Therefore, Brown does not anticipate each and every element of amended independent claim 1 under 35 U.S.C. § 102(e). Also, a *prima facie* case of obviousness under 35 U.S.C. § 103(a) cannot be established against amended independent claim 1 solely on the basis of the teachings of Brown. Accordingly, it is respectfully submitted that, under 35 U.S.C. §§ 102(e) and 103(a), amended independent claim 1 is allowable over Brown.

Claims 2-6, 8-10, and 68 are each allowable, among other reasons, as depending from claim 1, which is allowable.

In addition, claim 10 is allowable since Brown lacks any teaching, suggestion, or express or inherent description that the contact thereof may include a contact layer comprising "a material having a melting temperature that is greater than a temperature required to switch a phase change component in electrical communication with the contact between a plurality of states." In fact, Brown does not teach, suggest, or expressly or inherently describe that the contact disclosed therein may be positioned adjacent to a structure that includes a phase change component or that the semiconductor device disclosed therein could even include a phase change component.

Claim 68 is additionally allowable since Brown does not teach, suggest, or expressly or inherently describe that an intermediate conductive layer or an electrically conductive contact layer of the contact described therein may abut a silicon-containing structure. Rather, the Brown discloses that the copper contacts thereof are in contact with a photodefinable resin layer.

Further, it is respectfully submitted that one of ordinary skill in the art would not have been motivated by either Brown or the knowledge that was generally available in the art before the filing date of the above-referenced application to modify the teachings of Brown in the manner that has been asserted to render the subject matter recited in claim 68 unpatentable. Specifically, the copper conductive portions of the contact of Brown could not contact a silicon oxide-containing structure, as recited in claim 68, as proposed to be amended, since, as is well known to those of skill in the

art, copper reacts with silicon-containing materials in a manner that causes the copper to blister or delaminate from adjacent silicon-containing structures, such as structure formed from a silicon oxide or a glass.

For the same reason, it is respectfully submitted that there would have been no reason for one of ordinary skill in the art to expect that modifying the teachings of Brown in the asserted manner would have been successful. A copper contact cannot abut a silicon oxide-containing protective layer without resulting in blistering or delamination of the copper contact from the protective layer.

The teachings of Brown are not inconsistent with this well-known fact. As shown in FIG. 4, the copper layer 26 is clearly shielded from contacting the silicon-containing dielectric layer 11 by resin layer 14.

It, therefore, appears that modification of the teachings of Brown in the asserted manner could only have been based upon the benefit of hindsight provided by the subject matter disclosed and recited in the claims of the above-referenced patent application.

With respect to independent claim 32, as amended and presented herein, it is understood that, as a product-by-process claim, the only limitations considered by the Office in determining patentability thereof are the product limitations.

Amended independent claim 32 recites, among other things, a contact that includes "a contact layer and an intermediate conductive layer which partially contact one another and substantially envelop an insulator component . . ." The contact "contacting a structure located *at a lower level than* a silicon-containing dielectric layer of the semiconductor device so as to at least thermally insulate underlying structure." (Emphasis supplied).

It is respectfully submitted that Brown does not teach, suggest, or expressly or inherently describe a contact that contacts a structure located *at a lower level than* a silicon-containing dielectric layer of a semiconductor device. Rather, the teachings, suggestion, and description of Brown are limited to a contact that contacts a pad 12 which is located at the same level as a silicon-containing dielectric layer 11 of a semiconductor device and to contacts that are laterally offset from other structures of the semiconductor device. The mere statement at col. 4, lines 63-67,

of Brown that pads 12 may be located "anywhere" does not amount to a description, teaching, or suggestion of anything other than the embodiments that have been described therein with any amount of detail.

Further, Brown fails to teach, suggest, or expressly or inherently describe that the contact thereof may be positioned so as to at least thermally insulate the contacted structure.

Therefore, Brown does not anticipate each and every element of amended independent claim 32 under 35 U.S.C. § 102(e). Further, the teachings of Brown do not support a *prima facie* case of obviousness against amended independent claim 32, as required to maintain a rejection under 35 U.S.C. § 103(a). Accordingly, under 35 U.S.C. §§ 102 and 103(a), amended independent claim 32 is allowable over Brown.

Each of claims 33-38 and 70 is allowable, among other reasons, as depending from claim 32, which is allowable.

Claim 70 is additionally allowable since Brown does not teach, suggest, or expressly or inherently describe a contact with either an intermediate conductive layer or an electrically conductive contact layer that abuts a major surface of the silicon-containing dielectric layer of the semiconductor device. Rather, FIG. 4 of Brown illustrates that the copper layer 26 of the contact thereof only abuts an upper surface of resin layer 18, an edge of resin layer 14, and an upper surface of pad 12.

Further, it is respectfully submitted that one of ordinary skill in the art would not have been motivated by either Brown or the knowledge that was generally available in the art before the filing date of the above-referenced application to modify the teachings of Brown in the manner that has been asserted to render the subject matter recited in claim 70 unpatentable. Specifically, the copper conductive portions of the contact of Brown could not contact a silicon-containing dielectric structure, as recited in claim 70 since, as is well known to those of skill in the art, copper reacts with silicon-containing materials in a manner that causes the copper to blister or delaminate from adjacent silicon-containing structures, such as structure formed from a silicon oxide or a glass. For the same reason, it is respectfully submitted that there would have been no reason for one of ordinary skill in the art to expect that modifying the teachings of Brown in the asserted manner would have been successful. A copper contact cannot abut a silicon oxide-containing protective

layer without resulting in blistering or delamination of the copper contact from the protective layer. Again, the teachings of Brown are not inconsistent with these well-known facts. As shown in FIG. 4, Brown illustrates that the copper layer 26 does not contact the silicon-containing dielectric layer 11 but, rather, remains separated therefrom by way of a resin layer 14.

Therefore, it appears that modification of the teachings of Brown in the asserted manner could only have been based upon the benefit of hindsight provided by the subject matter disclosed and recited in the claims of the above-referenced patent application.

Accordingly, withdrawal of the 35 U.S.C. § 102(e) and 35 U.S.C. § 103(a) rejections of claims 1-6, 8-10, 32-38, 68, and 70 is respectfully requested.

Rejections Under 35 U.S.C. § 103(a)

Again, M.P.E.P. 706.02(j) sets forth the standard for a section 103(a) rejection:
To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Brown in View of Whitten

Claim 11 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Brown in view of U.S. Patent 5,451,811 to Whitten et al. (hereinafter "Whitten").

Claim 11 is allowable, among other reasons, as depending from independent claim 1, which is allowable.

In addition, it is respectfully submitted that one of ordinary skill in the art would not have been motivated by Brown, Whitten, or the knowledge that was generally available in the art to

combine the teachings of Brown and Whitten in the asserted manner. Specifically, Brown teaches an *external contact* for a semiconductor device, while the portion of Whitten that is relied upon is drawn to an *embedded upper electrode* of an antifuse.

For these reasons, it is respectfully requested that the 35 U.S.C. § 103(a) rejection of claim 11 be withdrawn.

Ovshinsky in View of Brown

Claims 7, 12-19, 39-54, 56-66, 69, and 71 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 5,296,716 to Ovshinsky et al. (hereinafter "Ovshinsky"), in view of Brown.

Ovshinsky teaches an electrically erasable programmable memory (EEPROM) that includes memory elements formed from a phase change material. The phase change material has a plurality of electrical conductivity states, depending upon whether the material is in an amorphous state, a crystalline state, or an intermediate state. The state of the material depends upon the amount of energy (*e.g.*, heat) applied to the memory element. Ovshinsky does not recognize heat loss as a problem or disclose contacts or other structures to at least thermally insulate the phase change memory elements of the EEPROM disclosed therein.

Claim 7 is allowable, among other reasons, as depending from claim 1, which is allowable.

Independent claim 12 recites a contact for a memory element that includes a phase change component. The contact includes, among other things, an intermediate conductive layer adjacent to and in electrical and thermal communication with the memory element.

Neither Ovshinsky nor Brown, taken alone or in combination, teaches or suggests a contact for a memory that includes an intermediate conductive layer adjacent to and in electrical and thermal communication with a memory element. Rather, Brown teaches a contact pad that is located adjacent to a bond pad. Ovshinsky teaches adjacent memory elements that are bridged, or electrically connected, to one another by way of an upper conductor 42. The upper conductor 42 is, in turn, covered with an encapsulant layer 44. Thus, Ovshinsky lacks any teaching or suggestion

that a contact pad, let alone a contact pad that includes the features recited in independent claim 12, may contact any of the memory elements thereof. Therefore, it is respectfully submitted that independent claim 12 is allowable over the combination of Ovshinsky and Brown.

Claims 13-19 are each allowable, among other reasons, as depending from claim 12, which is allowable.

Independent claim 39 recites an electrically erasable programmable memory device that includes, among other things, a memory element and a contact. The memory element includes at least one of an electrode and a memory cell that comprises a phase change material. The contact includes, among other things, an intermediate conductive layer positioned adjacent to and in electrical and thermal communication with the memory element, as well as an insulator component adjacent the intermediate conductive layer.

Ovshinsky and Brown both lack any teaching or suggestion of an electrically erasable programmable memory device that includes a memory element with an intermediate conductive layer of a contact positioned adjacent thereto and in electrical and thermal communication therewith. Rather, Brown teaches a contact pad that is located adjacent to a bond pad. The teachings of Ovshinsky are limited to a use of an encapsulated (by encapsulant layer 44) upper conductor 42 that bridges adjacent memory elements. Ovshinsky lacks any teaching or suggestion that any of the memory elements may be contacted by a contact, let alone a contact that includes the features recited in independent claim 39. Therefore, it is respectfully submitted that independent claim 39 is allowable over the combination of Ovshinsky and Brown.

Claims 40-44 are each allowable, among other reasons, as depending from claim 39, which is allowable.

Independent claim 45 recites a semiconductor device that includes at least one contact with, among other things, an intermediate conductive layer positioned adjacent to and in electrical and thermal communication with a structure of the semiconductor device that comprises a phase change component.

Neither Ovshinsky nor Brown, taken alone or in combination, teaches or suggests a semiconductor device with a contact that includes an intermediate conductive layer positioned adjacent to and in electrical and thermal communication with a structure of the semiconductor device that comprises a phase change component. Again, the contact of Brown is disposed against an underlying bond pad or conductive trace, while Ovshinsky teaches a device with memory elements that have an upper conductor 42 adjacent thereto. Therefore, it is respectfully submitted that claim 45, as proposed to be amended, is allowable over the combination of Ovshinsky and Brown.

Claims 46-54 are each allowable, among other reasons, as depending from claim 45, which is allowable.

Independent claim 56, as proposed to be amended herein, recites an enhanced electrically erasable programmable element with a contact that includes "an intermediate conductive layer positioned adjacent to and in electrical communication with the electrically erasable programmable element; an insulator component disposed adjacent said intermediate conductive layer and over the electrically erasable programmable element so as to insulate same; and an electrically conductive contact layer adjacent said insulator component."

Neither Ovshinsky nor Brown teaches or suggests an enhanced electrically erasable programmable element with a contact that includes an intermediate conductive layer positioned adjacent thereto and in electrical communication therewith. Moreover, neither Ovshinsky nor Brown teaches or suggests a contact that includes an insulator component and which is positioned over an electrically erasable programmable element so as to insulate the programmable element. Therefore, it is respectfully submitted that independent claim 56 is allowable over the combination of Ovshinsky and Brown.

Claims 57-66 are each allowable, among other reasons, as depending from claim 56, which is allowable.

Claim 69 is allowable, among other reasons, as depending from claim 1, which is allowable.

Claim 71 is allowable, among other reasons, as depending from claim 32, which is allowable.

Moreover, it is respectfully submitted that one of ordinary skill in the art, prior to the time at which the referenced application was filed, would not have been motivated to combine the teachings of Ovshinsky and Brown in the manner that has been asserted in the outstanding Office Action. Specifically, it is submitted that one of ordinary skill in the art would not have been motivated to combine with a memory element, an electrically erasable programmable element, or any other structure that includes a phase change component, a contact including an intermediate conductive layer, an insulator component, and a contact layer, with the intermediate conductive layer of the contact being positioned adjacent to and in electrical or thermal communication with the memory element or other structure, as is recited in independent claims 12, 39, 45, and 56.

While FIG. 4 of Brown depicts a conductive terminal positioned above a corresponding bond pad formed from a different conductive material, and the structure has a similar appearance to that shown in the figures of the referenced application, Brown does not provide any suggestion or motivation that the structure illustrated in FIG. 4 could be used adjacent a memory cell or other structure similar in type to that taught in Ovshinsky.

Furthermore, Ovshinsky, which discloses an EEPROM that includes phase change elements, would also have failed, prior to the time at which the referenced application was filed, to have provided any suggestion or motivation to one of ordinary skill in the art to dispose a contact of a type recited in the claims of the referenced application adjacent to a memory cell or other structure including a phase change component in such a manner that would thermally insulate the phase change element. In fact, Ovshinsky does not even recognize a need for thermally insulating the phase change elements of the EEPROM disclosed therein. Moreover, the figures of Ovshinsky do not depict discrete electrical contacts, such as the exposed contacts of Brown, in communication with each memory element, but rather an encapsulated conductive line that connects adjacent memory elements.

It is further submitted that the knowledge generally available in the art prior to the time the present application was filed would also have failed to provide one of ordinary skill in the art with any suggestion or motivation to combine the teachings of Ovshinsky with the teachings of Brown.

Accordingly, it is respectfully submitted that any motivation to one of ordinary skill in the art to combine the teachings of Brown and Ovshinsky could only be based on the hindsight provided by the disclosure and claims of the referenced application.

For these reasons, it is respectfully submitted that, under 35 U.S.C. § 103(a), claims 7, 12-19, 39-54, 56-66, 69, and 71 are allowable over the combination of Ovshinsky and Brown.

Ovshinsky, Brown, and Whitten

Claims 20, 55, and 67 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ovshinsky, in view of Brown and, further, in view of Whitten.

Claim 20 is allowable, among other reasons, as depending from claim 12, which is allowable.

Claim 55 is allowable, among other reasons, as depending from claim 45, which is allowable.

Claim 67 is allowable, among other reasons, as depending from claim 56, which is allowable.

It is further submitted that each of claims 20, 55, and 67 is allowable because Whitten does not remedy the aforementioned deficiencies of Ovshinsky, Brown, and the generally-available knowledge in the art with respect to the elements of independent claims 12, 45, and 56, respectively, that are lacking in Ovshinsky and Brown, as well as with respect to providing one of ordinary skill in the art with some motivation to combine the teachings of Ovshinsky and Brown in the manner that has been asserted.

In view of the foregoing, it is respectfully requested that the 35 U.S.C. § 103(a) rejections of claims 7, 11-20, 39-67, 69, and 71 be withdrawn.

CONCLUSION

It is respectfully submitted that each of claims 1-20 and 32-71 is allowable. An early indication of the allowability of these claims is respectfully solicited, as is an indication that the above-referenced application has been passed for issuance. If any issues preventing the allowance of the above-referenced application remain which might be resolved by way of a telephone conference, the Office is kindly invited to contact the undersigned attorney.

Respectfully submitted,

Brick G. Power
Registration No. 38,581
Attorney for Applicant
TRASKBRITT, PC
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

Date: January 20, 2003

Enclosure: Version with Markings to Show Changes Made

BGP/jml

Document in ProLaw

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please amend the claims as follows:

1. (Amended four times) A contact for a semiconductor device, comprising:

an intermediate conductive layer contacting and in electrical communication with a structure located [beneath] at a lower level than a silicon-containing dielectric layer of the semiconductor device;

an insulator component positioned adjacent said intermediate conductive layer so as to at least thermally insulate said structure; and

an electrically conductive contact layer adjacent said insulator component and in communication with said intermediate conductive layer.

32. (Amended four times) A contact for a semiconductor device including a contact layer and an intermediate conductive layer which partially contact one another and substantially envelop an insulator component, the contact contacting a structure located [beneath] at a lower level than a silicon-containing dielectric layer of the semiconductor device so as to at least thermally insulate the structure, the contact fabricated by the process comprising:

forming the intermediate conductive layer on a surface of the semiconductor device and in electrical thermal communication with an active device region of the semiconductor device;

depositing a dielectric layer on the intermediate conductive layer;

patterning said dielectric layer to define the insulator component;

forming the contact layer substantially over an exposed area of the insulator component and in electrical communication with the intermediate conductive layer;

patterning the intermediate conductive layer; and

patterning the contact layer.